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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,574	10/18/2001	Mark Anders	10559-481001	3811
45209	7590	04/10/2006	EXAMINER	
INTEL/BLAKELY 12400 WILSHIRE BOULEVARD, SEVENTH FLOOR LOS ANGELES, CA 90025-1030				PATHAK, SUDHANSU C
		ART UNIT		PAPER NUMBER
				2611

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,574	ANDERS ET AL.	
	Examiner	Art Unit	
	Sudhanshu C. Pathak	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on November 30th, 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-11, 14-17 and 19 is/are rejected.
- 7) Claim(s) 12, 13, 18 and 20 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on October 18th, 2001 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____

DETAILED ACTION

1. Claims 1-to-19 are pending in the application.

Response to Arguments

2. In response to the arguments regarding to Claims 1 & 10 the applicant's arguments filed on November 30th, 2005 have been fully considered but they are not persuasive.

Burleson discloses transmission of data over a communication bus so as to minimize the power dissipation (Page 444, Abstract, lines 1-16 & Introduction).

Burleson further discloses transitional signaling ((encoding) from level signaling to transition signaling) in combination with further encoding (type of code words per data bit) so as reduce the switching activity on the bus thus minimizing the power consumption in the bus system (Page 445, left-hand column, Sec. "Level Signaling and Transition Signaling", lines 8-25 & Page 445, right-hand column, Sec. "Level Signaling and Transition Signaling", lines 1-20). Burleson also discloses transitional signaling (encoding) to be in response to a transition of the data (bit) between a current clock cycle and a previous clock cycle (Page 445, right-hand column, lines 1-25 (modulation equation)).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5, 10-11, 14-15 & 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art in view of Burleson et al. (Low-Power Encodings for Global Communication in CMOS VLSI; IEEE Transactions on Very Large Scale Integration (VLSI) Systems; Vol. 5, No. 4; Dec. 1997; Pages 444-455).

Regarding to Claims 1-5, 10, 14-15 & 19, the Applicant Admitted Prior Art (AAPA) discloses transmitting data over a dynamic bus thus reducing the effect of the parasitic miller capacitor effect (Specification, Page 1, Paragraph 2 & Specification, Page 2, Paragraphs 2-3). However, the AAPA does not specify encoding the data in response to the transition of the data between a current clock cycle and a previous clock cycle and then transmitting the encoded data on the bus.

Burleson discloses transmission of data over a communication bus so as to minimize the power dissipation (Page 444, Abstract, lines 1-16 & Introduction). Burleson further discloses transitional signaling ((encoding) from level signaling to transition signaling) in combination with further encoding (type of code words per data bit) so as reduce the switching activity on the bus thus minimizing the power consumption in the bus system (Page 445, left-hand column, Sec. "Level Signaling and Transition Signaling", lines 8-25 & Page 445, right-hand column, Sec. "Level Signaling and Transition Signaling", lines 1-20). Burleson also discloses transitional signaling (encoding) to be in response to a transition of the data (bit) between a current clock cycle and a previous clock cycle (Page 445, right-hand column, lines 1-25 (modulation equation)). Burleson also discloses a method of decoding the

encoded signal by comparing the first encoded signal received at the output in the current clock cycle to a second encoded signal received at the output in the previous clock cycle wherein the decoded signal comprises an output data signal having a value corresponding to the value of the input data (Page 445, right-hand column, lines 1-25 (demodulation equation)). Burleson further discloses a state machine implemented to implement an encoder (Fig. 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Burleson teaches that transition signaling for transmitting data over a data bus and this can be implemented in the bus as described in the AAPA so as to provide a simpler one-to-one context independent data for further encoding (code words) so as to minimize power consumption in the transmission of data over a dynamic bus. It would also have been obvious to one of ordinary skill in the art at the time of the invention that the comparing operation is performed by an exclusive-OR gate (operation). Furthermore, Burleson also teaches encoding NRZ data (level signaling) into a transition signaling data so as to avoid the complexity (and accuracy) of clock synchronization of the transmitted data in the receiver and further providing the interface to be integrated on the single chip in the transceiver. Furthermore, there is no criticality in the first encoded signal to be a HIGH signal and the second encoded signal comprising to be a LOW signal, this is a matter of design choice in terms of the initial data to be transmitted and the initial condition of the manchester encoder. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention that a decoder is implemented with a state machine so as to track

the output of the decoder for use in further decoding as is done while encoding the data.

Regarding to Claim 11, the AAPA in view of Burleson discloses a bus line having an input node operative to receive a data signal and an output node; a clock signal generator operative to generate a clock signal in a clock cycle; an encoder coupled to the input node and the clock signal generator, said encoder operative to generate an encoded signal in response to a transition at the input node between the current clock cycle and a previous clock cycle; and a decoder coupled to the output node and the clock signal generator as described above. Burleson further discloses a for encoding storing and accessing the data (Page 451, right-hand column, Sec. "Implementation of Coding in Space and Time", lines 7-9). Burleson further discloses implementing a shift register so as to store the data to be transmitted (Page 451, right-hand column, Sec. "Implementation of Coding in Space and Time", lines 15-21). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Burleson teaches implementing a shift register so as to store the input data and this can be implemented in the bus as described in AAPA so as to encode the data to minimize power consumption in the transmission of data over a dynamic bus, thus satisfying the limitations of the claims.

5. Claims 6-9 & 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art in view of Burleson et al. (Low-Power Encodings for Global Communication in CMOS VLSI; IEEE Transactions on Very

Large Scale Integration (VLSI) Systems; Vol. 5, No. 4; Dec. 1997; Pages 444-455) in further view of Schaire (4,453,229).

Regarding to Claims 6-9 & 16-17, the AAPA in view of Burleson discloses a method for transmitting encoded data over a dynamic bus wherein the data is encoded as a transitional signaling data and the decoding is performed by comparing the first encoded signal and the previous encoded signal as described above. However, storing and tracking the encoded signal at the receiver.

Schaire discloses a buffer and a shift register in the receiver so as to store and track the received data over a data bus (Fig. 1, elements 36, 38, 80 & Column 4, lines 1-28, 37-68). Schaire further discloses implementing flip-flops as storage devices (Column 2, lines 50-60). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Schaire teaches implementing a receiver buffer and shift register to store and track the data received over the bus, thus satisfying the limitations of the claim. Furthermore, there is no criticality in storing the received data before or after or before and after the decoding of the received data depending on the component complexity and accuracy requirements of the receiver, it is a matter of design choice. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention that a shift register is implemented by connecting multiple of flip flops in series so as to avoid timing issues in the received data.

Allowable Subject Matter

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6. Claims 12-13, 18 & 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

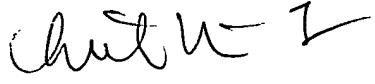
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (571)-272-3038. The examiner can normally be reached on M-F: 9am-6pm.

- If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571)-272-3042

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- The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.
- Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sudhanshu C. Pathak



CHIEH M. FAN
SUPERVISORY PATENT EXAMINER